

ABSTRACT OF THE DISCLOSURE

An interpretation flow, a translation and optimization flow, and an original instruction prefetch flow are defined independently of one another. A processor is realized as a chip multiprocessor or realized so that one instruction execution control unit can process a plurality of processing flows simultaneously. The plurality of processing flows is processed in parallel with one another. Furthermore, within the translation and optimization flow, translated instructions are arranged to define a plurality of processing flows. Within the interpretation flow, when each instruction is interpreted, if a translated instruction corresponding to the instruction processed within the translation and optimization flow is present, the translated instruction is executed. According to the present invention, an overhead including translation and optimization that are performed in order to execute instructions oriented to an incompatible processor is minimized. At the same time, translated instructions are processed quickly, and a processor is operated at a high speed with low power consumption. Furthermore, an overhead of original instruction fetching is reduced.

TOKYO 20050100000000000000000000000000